



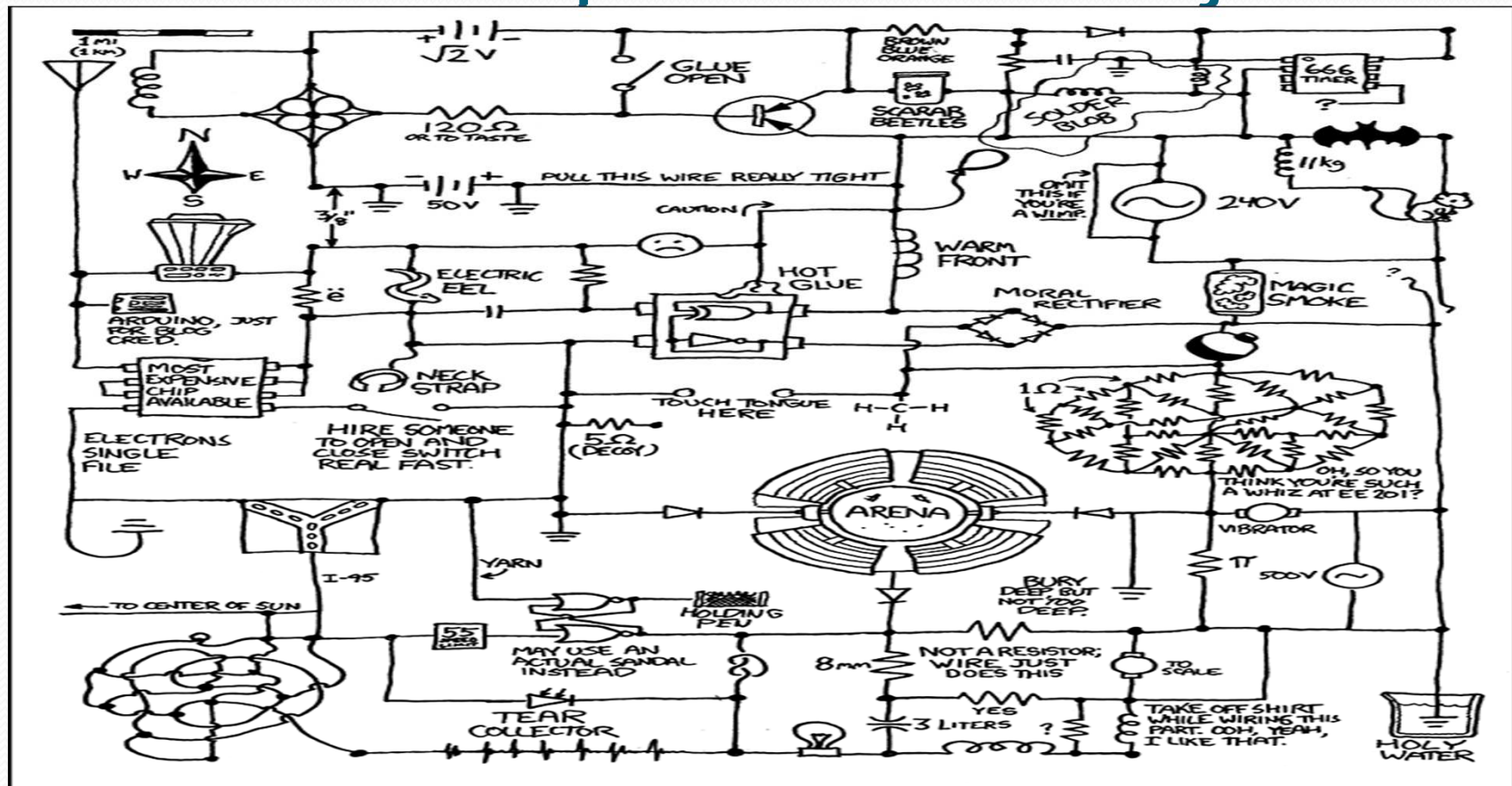
# High Performance Software Defined Radio

## Overview and Current Status

Warren Pratt, NROV  
John Westmoreland, AJ6BC



# What is the OpenHPSDR Project... ?





# What is the OpenHPSDR Project... ?

The OpenHPSDR Project is a modular, open source hardware and software platform for development of all components of a Software Defined Radio.

It is also a group of volunteers dedicated to the building of a pool of open-source Software Defined Radio design information.



# What is an OpenHPSDR radio?

*H*igh *P*erformance *S*oftware *D*efined *R*adio

An OpenHPSDR radio has the following features:

- Very High Performance
- Based upon an open source model (OHL/NCL hardware, GPL software)
- Generally modular and expandable
- Advances the State of the Radio Art



# TAPR's MISSION

Support OpenHPSDR development with:

R&D funding

- Breadboard prototypes
- Alpha PCBs

Early volume production

- Put leading edge technology into many hands



# TAPR's MISSION

Result: An ever growing pool of contributors,  
experimenters and subsequent advancement of the  
radio art

**OpenHPSDR and TAPR are separate entities**

**but:**

**They complement each other**

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# VK6RIO Chirp Beacon

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# VK6RIO Chirp Beacon

**What is it?**

**Weak signal beacon for ionospheric probing**

**Test path:**

**VK6 (Western Australia) to ZS6 (South Africa)**

Thanks to: Phil, VK6PH

Andrew VK3OE

Bob, VK4XV





# VK6RIO Chirp Beacon

## How does it work?

- TX at one end of path, RX at the other
- Sweep TX frequency over 2 kHz in 1 second
- Sweep RX over same frequency and interval
- Synchronize both TX and RX with GPS



# VK6RIO Chirp Beacon

## Theoretical Performance

A signal 36dB below the noise floor in a 2kHz bandwidth is detectable

This is 10dB better than any digital mode

If we increase the integration time from 2 to 60 seconds, we improve S/N by another 17dB



# VK6RIO Chirp Beacon

**On-air Test, 30 Jan 2014**

At VK6PH

Transmits 2kHz / 1s chirp signal towards VK4XV on 15m

At VK4XV

Signal not visible on panadapter or waterfall

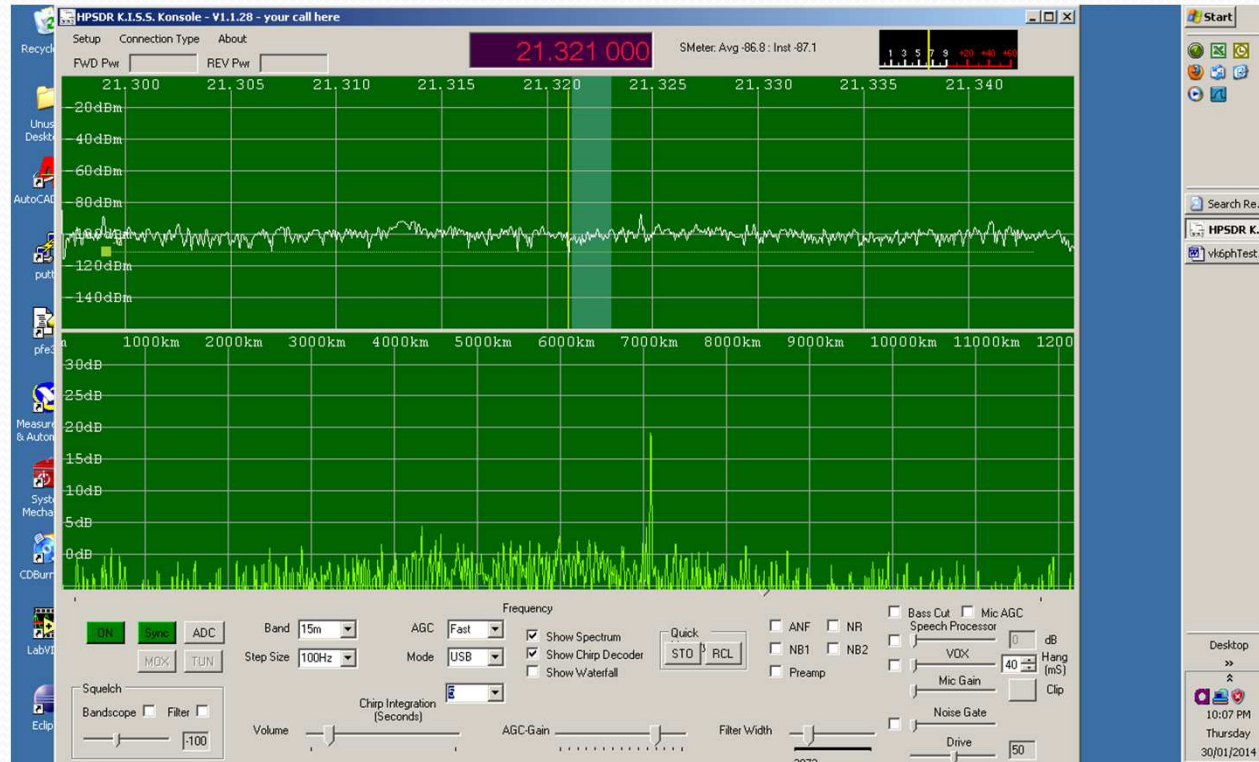
Signal not audible in receiver

Chirp decoder detects signal at 20dB over noise

No signals anywhere else on 15m band



# VK6RIO Chirp Beacon



Bandscope and chirp decoder screen shot  
Note that VK6PH was running 2mW at the time!



# VK6RIO Chirp Beacon

## Other observations

- 'Blip' on chirp decoder indicates TX to RX distance
- Calibration depends on exact time/freq synchronization
- Callsign can be encoded using sweep direction (1 bit/s)
- Wider frequency or longer sweep yields better S/N

## EME with simple antennas?



# Khronos

## GPS-disciplined Frequency Standard

Project leader is John, AJ6BC



# Khronos

- Compensated Crystal Oscillator (GPSTCXO) based timing/frequency reference for HPSDR.
- The purpose of KHRONOS is to provide:
  - 1PPS GPSDO Signal
  - 10MHz GPSDO Clock
  - ‘Calibration-Free’ (under most circumstances) operation



# Khronos - Features

- Plugs into Atlas Bus
- GSPDO Options:
  - GPSTCXO (OCXO option) from Jackson Labs
  - LC\_XO (OCXO option) from Jackson Labs
  - Themis (openHPSDR Design with add'l xOCXO Options)
- 10MHz Output For Atlas Bus
- I2C Atlas Bus Interface
- USB Interfaces for GPS and MSP-430 microcontroller
- LCD Interface – std or optional touch-screen





# Khronos - Features

- micro-SD Card for firmware upgrade storage, etc.
- Dual-Mode BlueTooth Radio (BLE 4.0 Enabled) that will allow for custom 'app' creation.
- USB Li-Ion (Single-cell) Charger for 14500 (AA) Li-Ion Cells
- Can be optionally powered via Power Pole connectors
- 3 On board temperature monitoring points plus addition of 2 optional NTC thermistor 'flying probes'
- Run time options can be set via ezLCD touchscreen.



# Khronos

- Status: currently in layout.
- Please see the Wiki page for the Khronos schematic:  
<http://openhpsdr.org/wiki/index.php?title=GPSTCXO>



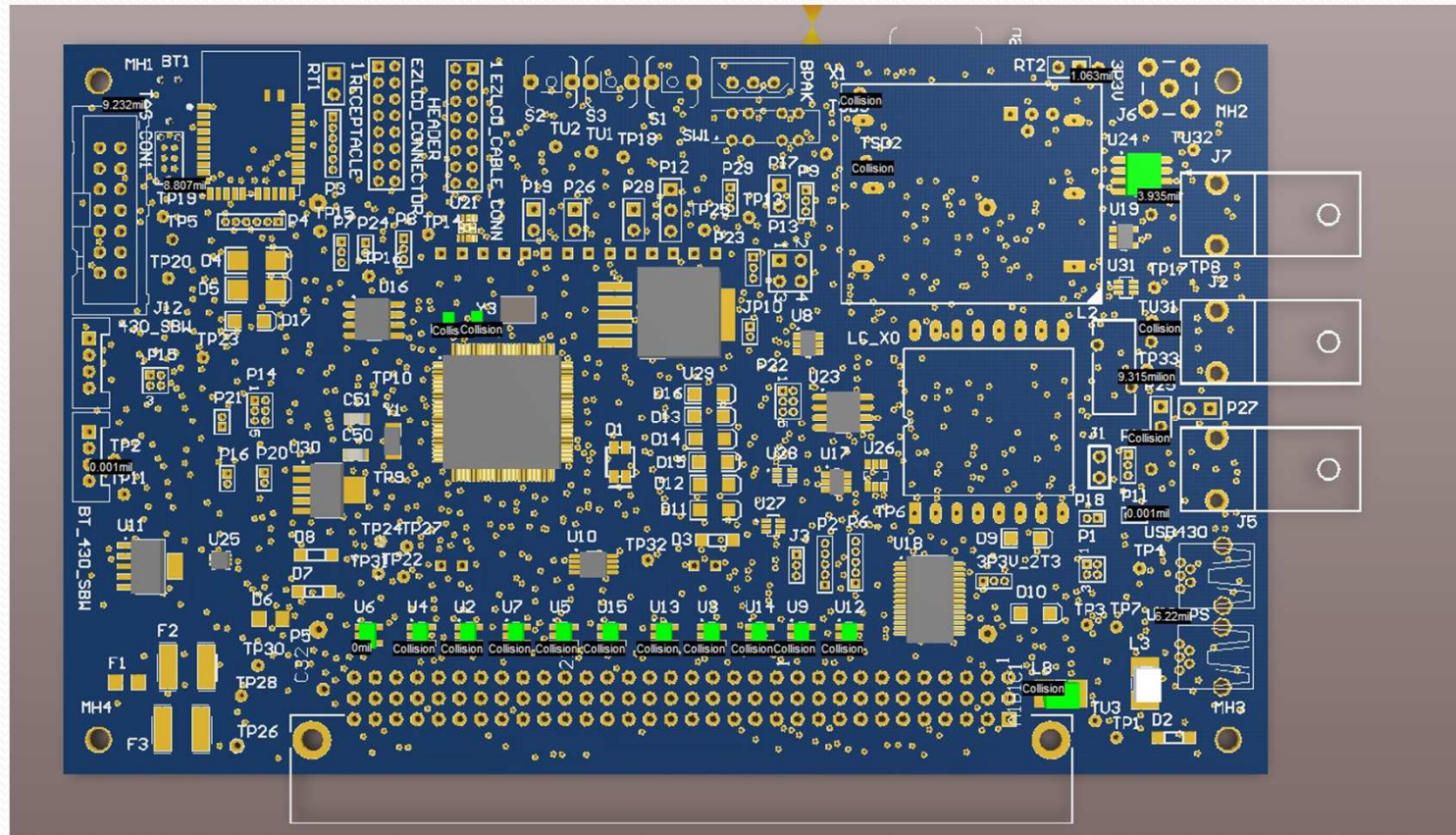
# Khronos

KHRONOS BLOCK DIAGRAM





# Chronos





# Themis

GPS-disciplined Frequency Standard Experimenter's Board

Project leader is John, AJ6BC.



# Themis

- Themis is an HPSDR GPS disciplined oscillator (GPSDO) design that is an **experimental** approach for disciplining Crystal Oven (OCXO) OCXO's and provides 1PPS, 10MHz, and GPS Timestamping to the Atlas Bus for the HPSDR System.
- Four OCXO's are currently supported - the MTI-Milliren 270 and 220, the Microcrystal OCXO, the ONYX IV from Wenzel, and the 3.3V ISOTEMP OCXO.
  - Most popular OCXO pin outs including standard Vref and EFC pins.



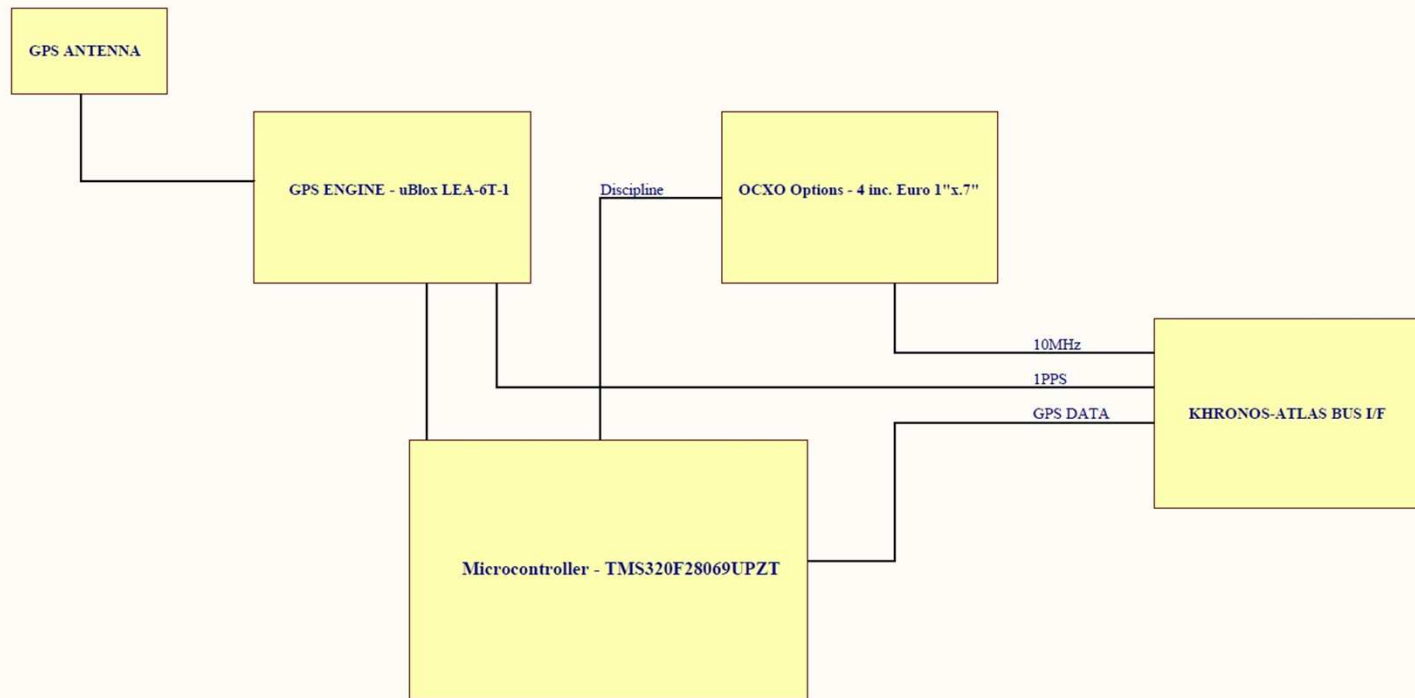
# Themis

- An on-board DSP provides the disciplining algorithms ('modified DLL' – digitally locked loop) plus will allow experimentation with custom algorithms.
- The GPS engine is the LEA-6 from u-Blox.
- Themis plugs into Khronos as an option to the other GPSSDO options.
  
- Status: Currently in layout.
- Please see the Wiki Page for the Themis schematic:  
<http://openhpsdr.org/wiki/index.php?title=GPSTCXO>



# Themis

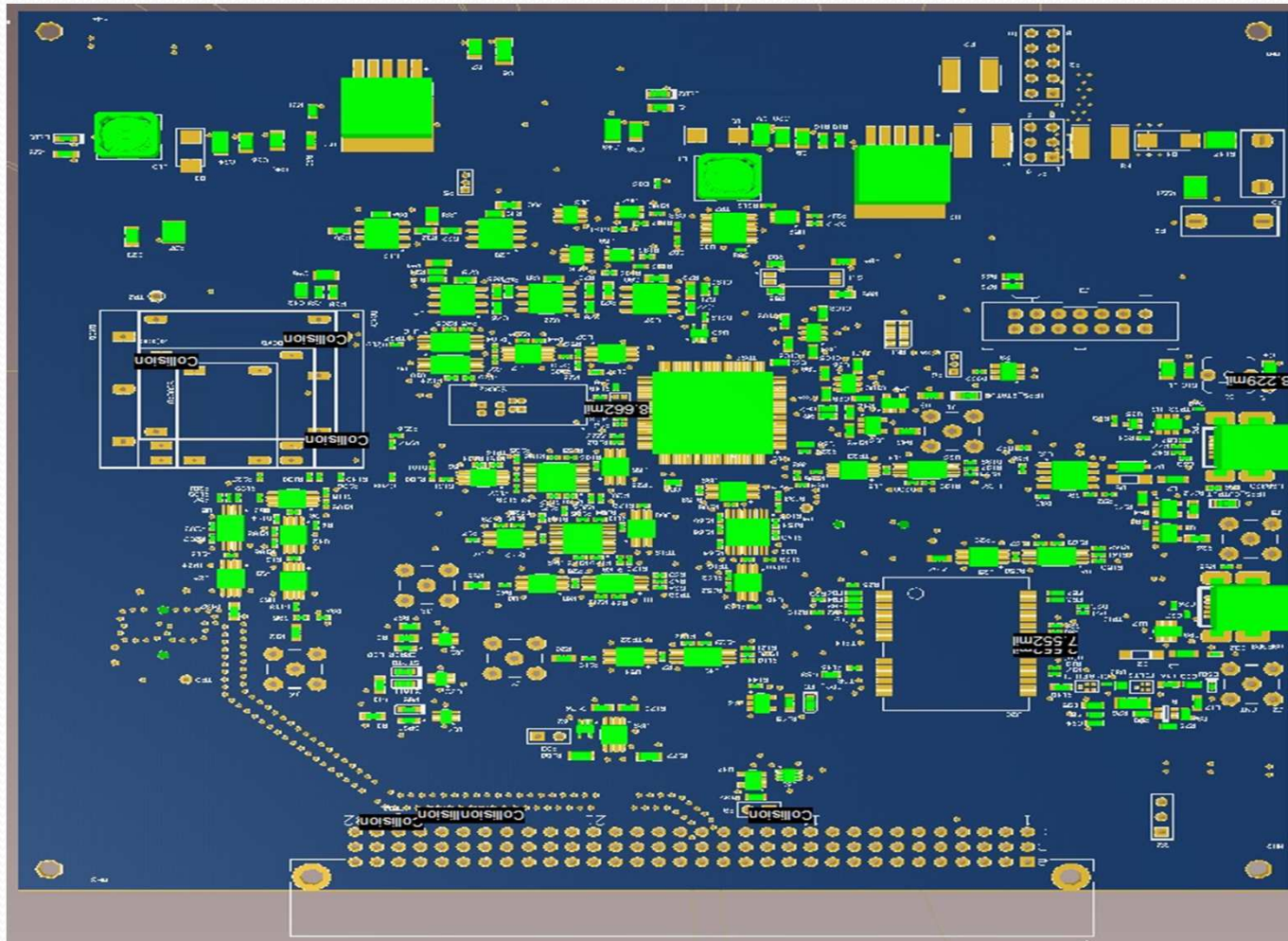
THEMIS BLOCK DIAGRAM







# Themis



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# Gen2 Hardware

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# Gen2 Hardware

## Gen2 Hardware Goals

- Extend useful life of Gen1 boards (Mercury, Pennylane)
- Increase performance of existing Gen1 boards
- Create new Gen2 high-performance boards
- Allow mixing of Gen1 and Gen2 boards in a system



# Gen2 Hardware

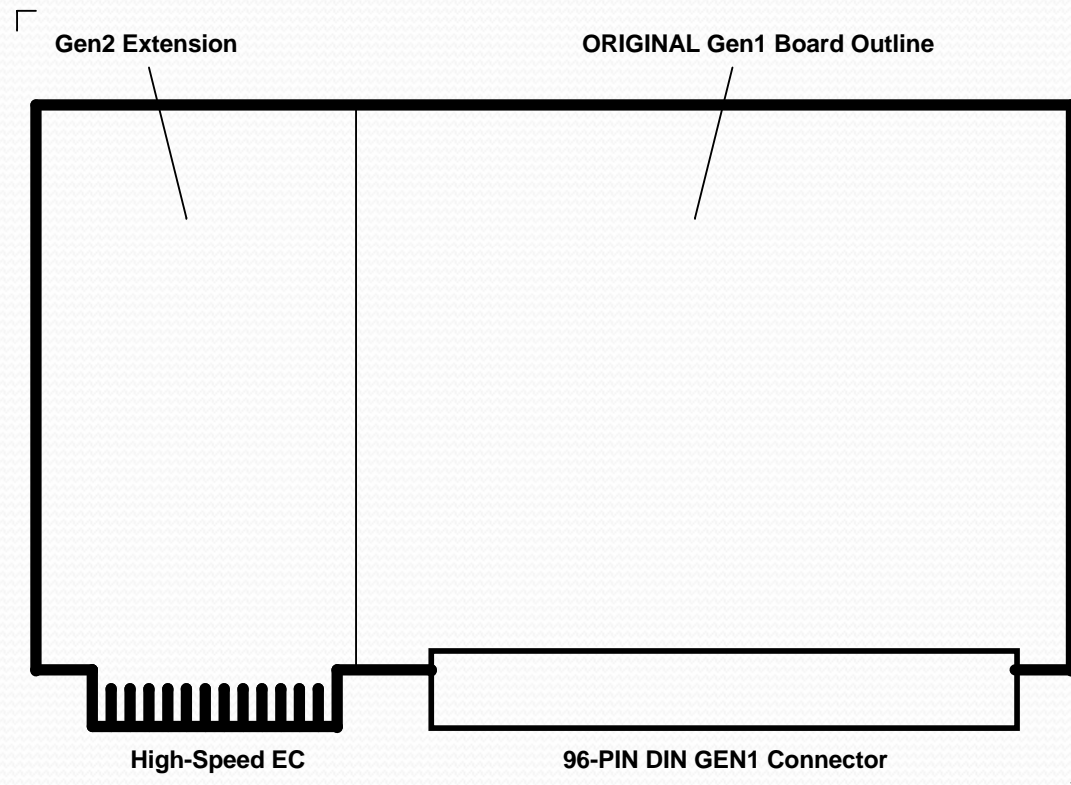
## Gen2 Architecture Changes

- Eliminate Atlas bottleneck: change bus → star topology
- Keep Atlas DIN connector, buffer signals at each
- Add high-speed Expansion Connector (EC) for Gen2
- Use LVDS, CML, 8B/10B encoding on EC for speed
- Add common hardware to baseboard



# Gen2 Hardware

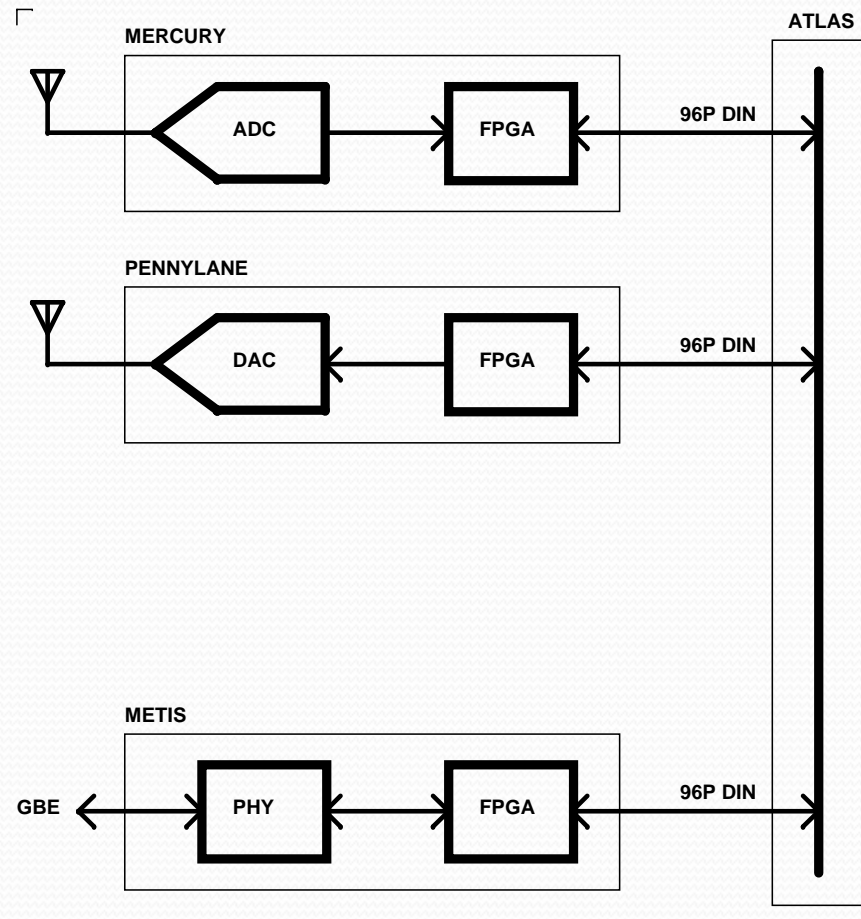
## Proposed Gen2 Board Outline





# Gen2 Hardware

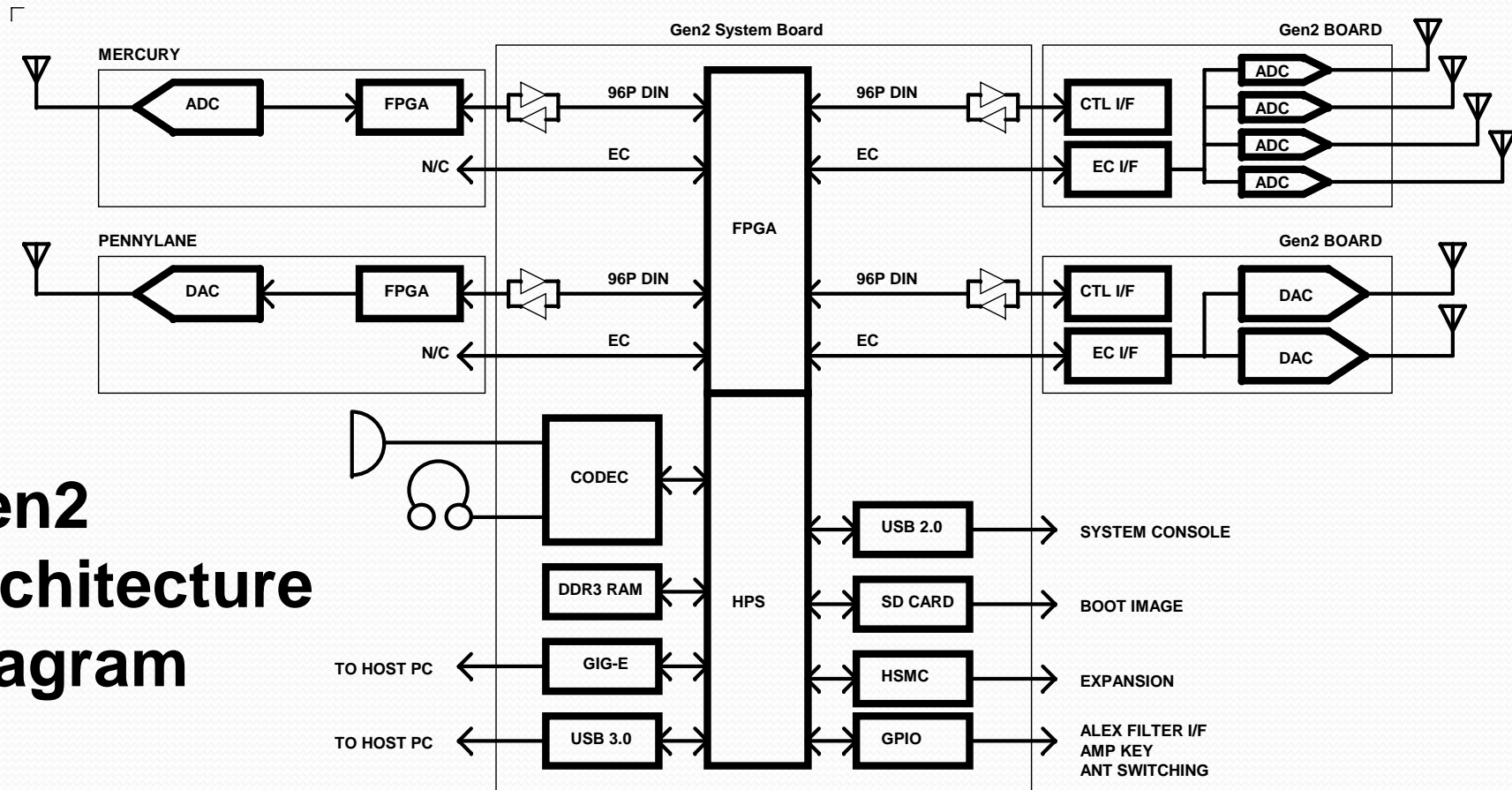
## Gen1 Architecture Diagram





# Gen2 Hardware

## Gen2 Architecture Diagram





# Gen2 Hardware

- **Medusa** Receiver: four 16b@122.88Msps ADCs
- **OctoMerc** Receiver: eight 16b@122.88Msps ADCs
- **The Flash** High-speed RX: two 12b@2.5Gsps ADCs
- **Strawberry Fields** TX: four 16b@1.0Gsps DACs



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# Direct CW

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# Direct CW

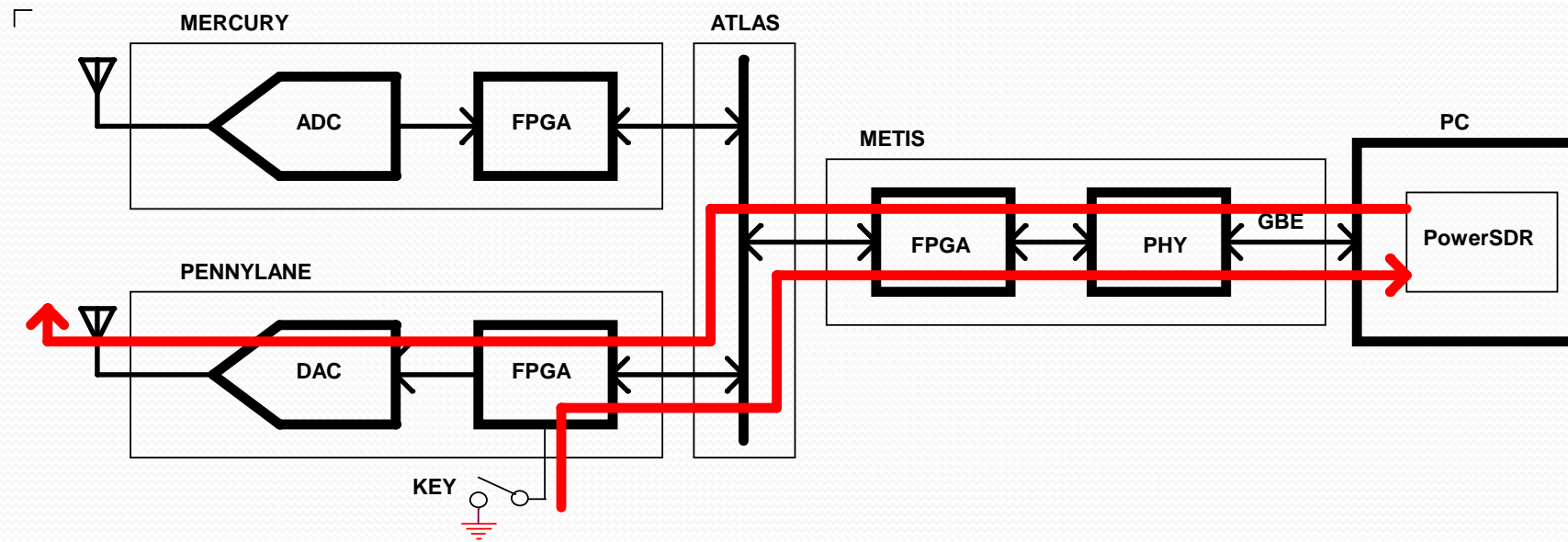
Problem: PowerSDR™ latency is too long to permit full-break-in CW operation at reasonable sending speeds

Solution: Implement the CW transmitter within the FPGA, eliminating the software and communications delays



# Direct CW

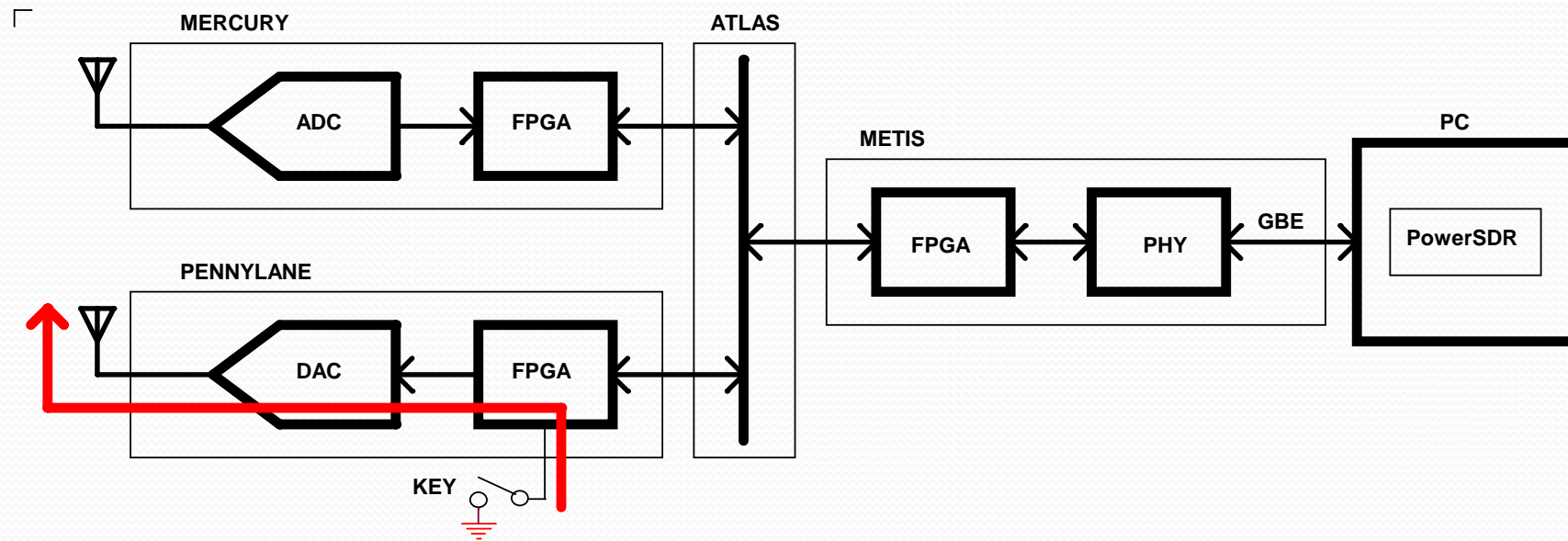
How we do it now





# Direct CW

## Improved method



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# Metis Gigabit Ethernet



# Metis Gigabit Ethernet

- Metis/Hermes hardware supports 10/100/1000 Mb/s
- Current FPGA code runs interface at only 100 Mb/s

VE3NEA and VK6PH are re-organizing the FPGA code and are adding support for 1000 Mb/s (Gigabit Ethernet)

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# Cyclops 6GHz SA

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# New & Improved Cyclops

## 6 GHz Spectrum Analyzer

- ❑ New MAX2870 device evaluated, range 27 MHz to 6 GHz
- ❑ Use down conversion with low-IF (40-50MHz)
- ❑ Tested and proved multiple LO + IF technique to cancel images
- ❑ Proto using Metis/Mercury, MAX2870 EVB and KISS Konsole
- ❑ Required multiple RX “stitching” implemented in PowerSDR
- ❑ Next stage is PCB layout for Alpha version

### Status:

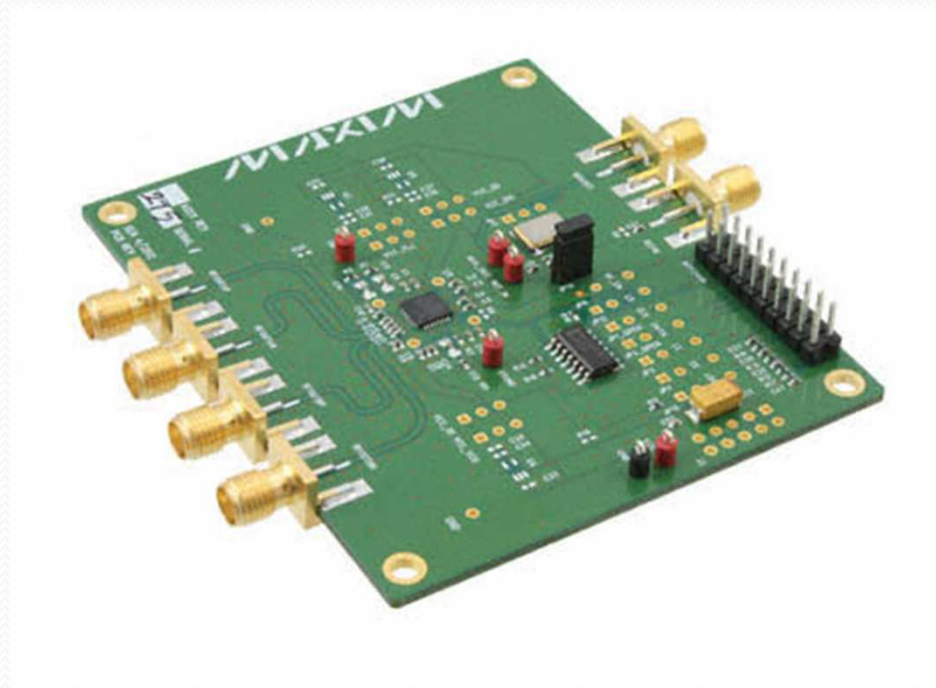
Project leaders: Phil, VK6PH and Berndt, VK5ABN

Ready to begin PCB layout





# New & Improved Cyclops



MAX2870 Evaluation Board

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# Hermes VNA

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# Vector Network Analyzer

## Hermes-based VNA

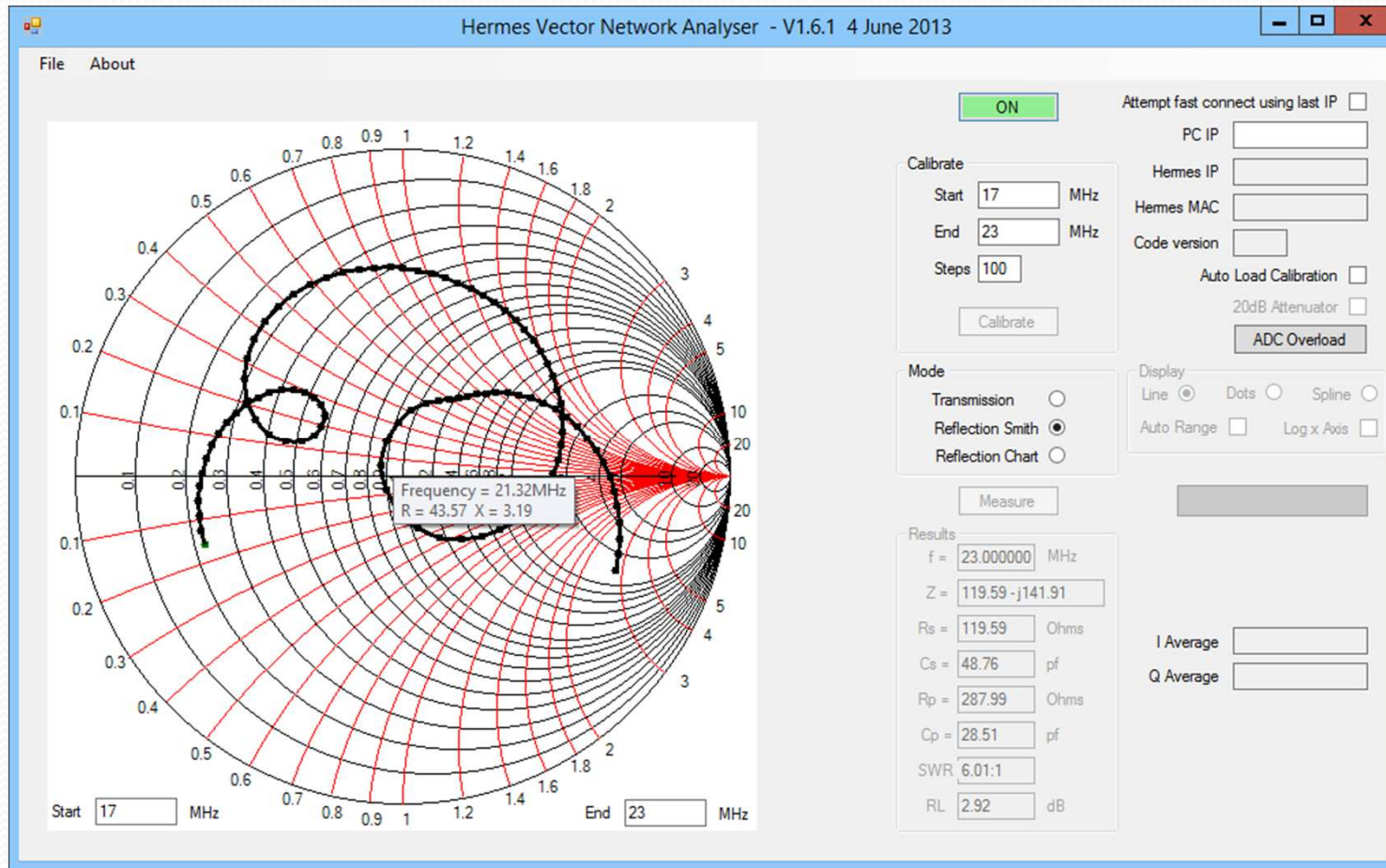
- ❑ Support built in to Hermes FPGA code
- ❑ Two software versions available: VK6PH and VE3NEA
- ❑ Both PC software versions released under GPL
- ❑ FPGA code improvements by VE3NEA have reduced scan times
- ❑ Reflection or Transmission VNA
- ❑ Requires external bridge for reflection measurements
- ❑ 100kHz to 60MHz in 1kHz steps
- ❑ Working on port to Apache Labs Angelia/Anan boards

### Status:

Project leaders: Phil, VK6PH and Alex, VE3NEA  
FPGA code for Angelia/Anan in progress



# Hermes VNA

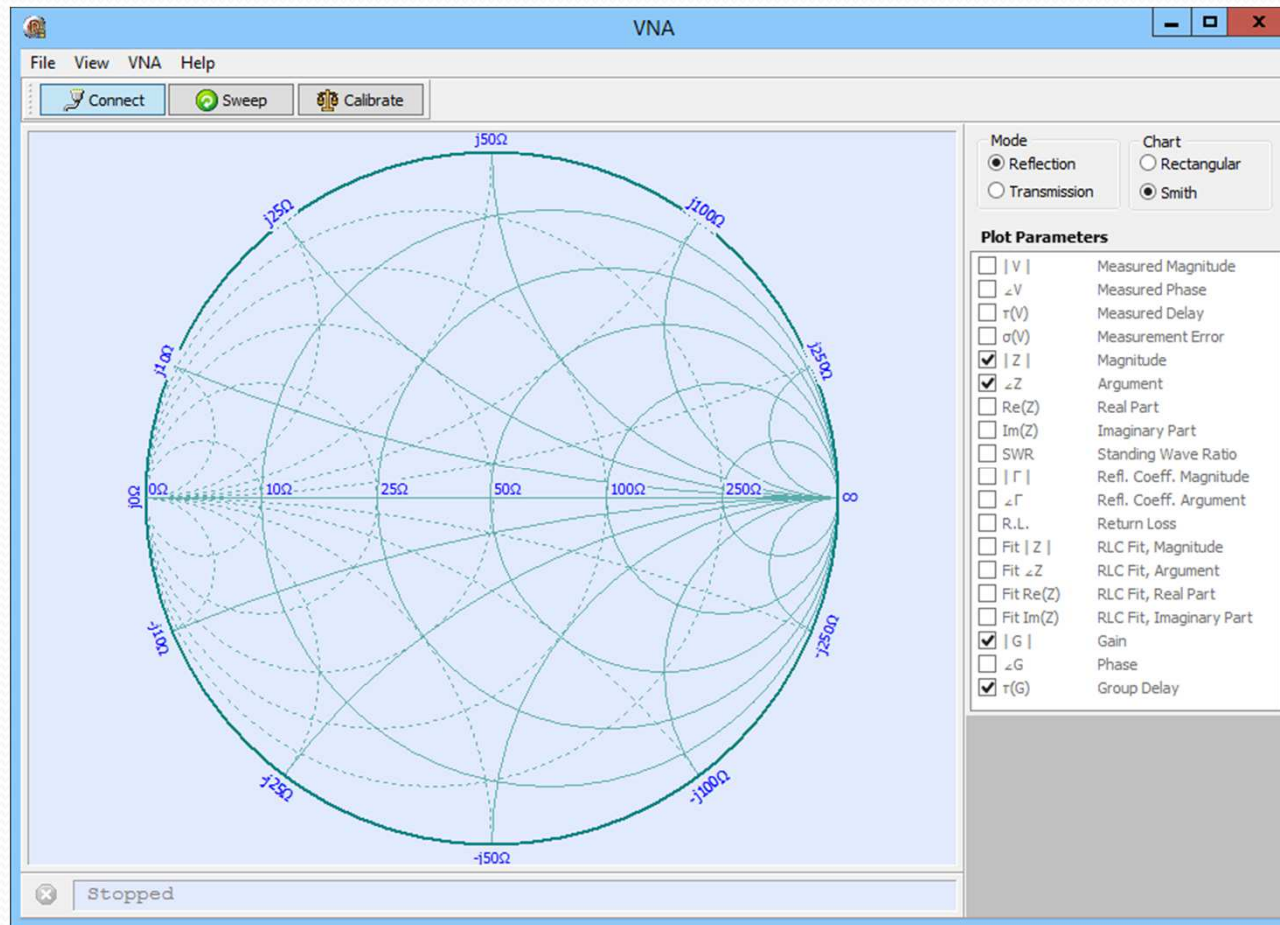


VK6PH VNA Software



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# Hermes VNA



VK6PH VNA Software

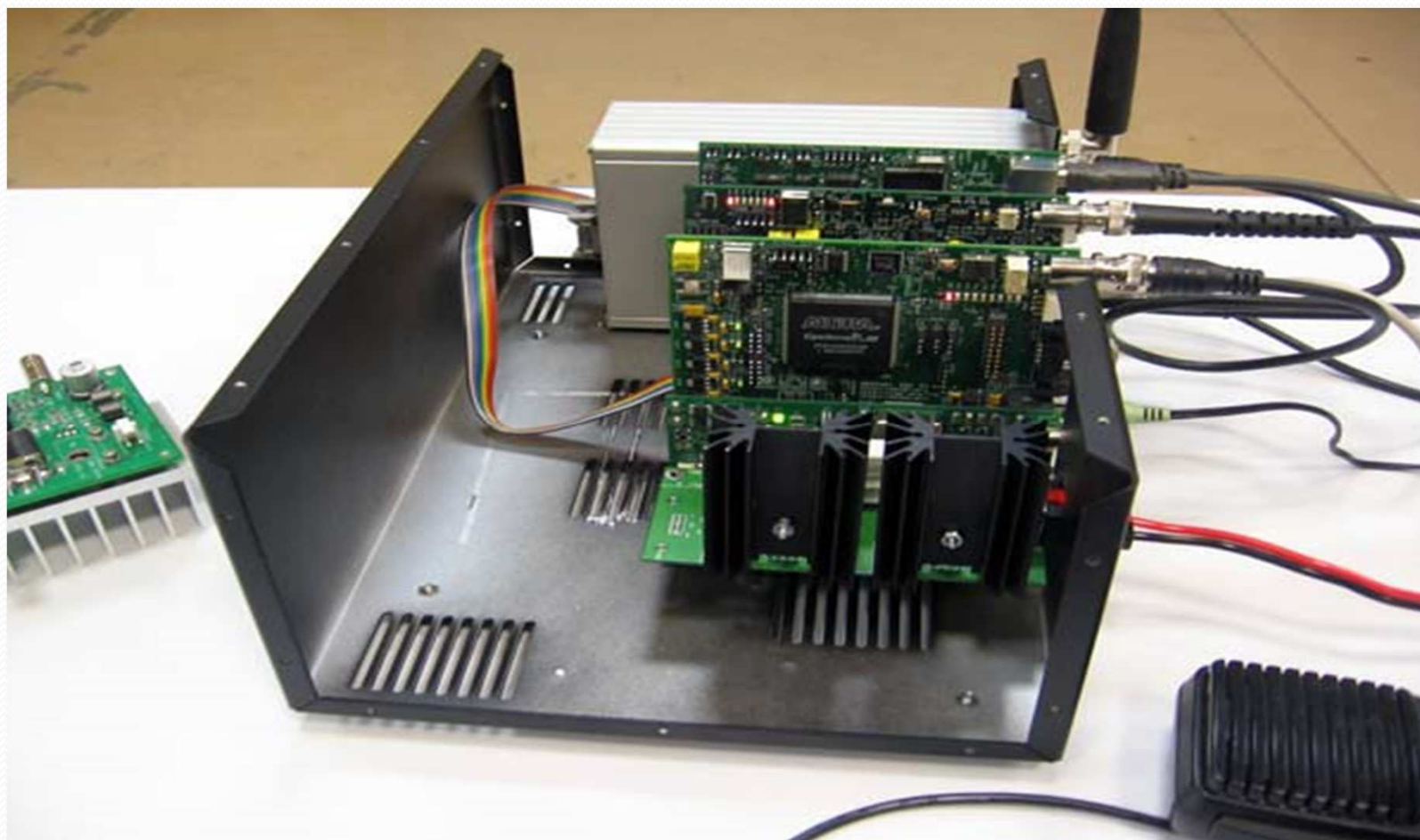


## Some OpenHPSDR Rig Pictures





## Some OpenHPSDR Rig Pictures





## Some OpenHPSDR Rig Pictures







## Some OpenHPSDR Rig Pictures





# Some OpenHPSDR Rig Pictures





## Some OpenHPSDR Rig Pictures





## Some OpenHPSDR Rig Pictures





# Thank you!

openHPSDR Project information at:

[www.openhpsdr.org](http://www.openhpsdr.org)

openHPSDR Article in May/June 2014 QEX:

[The High Performance Software Defined Radio Project,  
Scotty Cowling, WA2DFI plus other SDR articles this yr.](#)

Boards available at:

[www.tapr.org](http://www.tapr.org)



# References

1. D.W. Allan, L. Fey, H.E. Machlan, J.A. Barnes, “An Ultra-Precise Time Synchronization System Designed By Computer Simulation”, **Frequency**, Radio Standards Laboratory, National Bureau of Standards, Boulder, Colorado, Jan. 1968.
2. Bill Bourke and Bruce Penrod, “An Analysis of a Microprocessor Controlled Disciplined Frequency Standard”, **Austron, Inc.**, 37<sup>th</sup> Annual Symposium On Frequency Control, IEEE, June 1983.

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# Questions?

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